REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 3, 2002, and the references cited therewith.

Claims 1, 6, 13, and 18 are amended, no claims are canceled, and no claims are added; as a result, claims1-50 remain pending in this application.

§102 Rejection of the Claims

Claims 6-24 were rejected under 35 USC § 102(e) as being anticipated by Rengarajan et al. (U.S. Patent No. 6,323,103).

Applicant does not admit that Rengarajan is indeed prior art and reserves the right to swear behind this reference at a later date. Nevertheless the Applicant believes that the present invention is distinguishable from the reference for the following reasons.

The rejection states:

> Rengarajan et al. teach a method of forming a first gate dielectric layer 12 on a semiconductor substrate 10 , forming a first conductivity type semiconductor layer 14 on top of the first gate dielectric layer 12 , selectively removing a portion of the first conductivity type semiconductor layer 14 to expose the first gate dielectric 12, the portion defining a first conductivity type well region, forming a first conductivity type semiconductor well 30 in the first conductivity type well region, removing the first gate dielectric layer 12 in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well, forming a second gate dielectric layer 12' over the exposed portion of the first conductivity type semiconductor well 30 , depositing a second conductivity type semiconductor layer 34 on the second gate dielectric layer 12', and forming a second conductivity type gate 44 from the second conductivity type semiconductor layer and forming source/drain regions 48 adjacent the gate.

Rengarajan appears to show forming a second gate dielectric layer 12' over an exposed portion of a semiconductor well. However, Rengarajan does not show, teach, or suggest modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material. Rengarajan merely shows forming a gate dielectric 12', which from the drawings, appears to be formed from the same material as gate dielectric 12, and which appears to be formed to the same thickness as gate dielectric 12. Rengarajan also does not show, teach, or suggest forming a second gate

dielectric layer that differs in thickness from the first gate dielectric layer. Rengarajan also does not show, teach, or suggest coupling a hardened dielectric layer to the second gate dielectric layer.

In contrast, Applicant's amended claims 1 and 13 include modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material. Further Applicant's amended claims 6 and 18 include forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well, the second gate dielectric layer being adapted for operation with a second conductivity type gate material. Further, Applicant's claims 8 and 20 include coupling a hardened dielectric layer to the second gate dielectric layer. Further, Applicant's claims 9 and 21 include a second gate dielectric layer that differs in thickness from the first gate dielectric layer.

Because the Rengarajan reference does not show every element of Applicant's claims, a 35 USC § 102(e) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 1, 6, 13, and 18 as amended. Further, reconsideration and withdrawal of the rejection is respectfully requested with respect to claims 8, 9, 20, and 21 on their own grounds as outlined above. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims as depending on allowable base claims.

§103 Rejection of the Claims

Claims 1-5 and 13-17 were rejected under 35 USC § 103(a) as being unpatentable over Rengarajan et al. in view of Choi et al. (U.S. Patent No. 5,750,424).

Applicant respectfully submits that the Choi reference does not cure the deficiencies of Rengarajan as asserted under 102(e) arguments above. Applicant reserves the right to further argue the Choi reference at a later date.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with

respect to Applicant's independent claims 1, 6, 13, and 18. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 19 day of December, 2002.

Tina Kohat
Name

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Signature